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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,575	06/30/2003	Tae Yun Kim	40296-0006	7309

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EXAMINER
TSAI, SHENG JEN

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	**Applicant(s)**
Office Action Summary	10/608,575	KIM, TAE YUN
	Examiner	**Art Unit**	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2005*.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

   4a) Of the above claim(s) *3-5 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7,12,14 and 19-23* is/are rejected.

7)☒ Claim(s) *8-11,13 and 15-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☒ All   b)☐ Some * c)☐ None of:

   1.☒ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This Office Action is taken in response to Applicants' Amendment and Remarks

filed on December 16, 2005 regarding application 10/608,575 filed on June 30, 2003.

2.   Claims 1-23 are pending in the application under consideration.

Claims 1, 2, 6, 7, 9 and 12-18 have been amended.

Claims 3-5 and 20 have been cancelled.

Claims 21-23 have been added.

3.   ***Response to Amendments and Remarks***

Applicants' amendments and remarks have been fully and carefully considered.

In response, another round of claim analysis based on the reference relied on

previously (Hwang et al., US 6,590,822) has been embarked. Refer to the

corresponding sections of the claim analysis for details.

Double Patenting

4.   The nonstatutory double patenting rejection is based on a judicially created

doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent

and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225

USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*,

418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5.   Claims 1-2, 6-7, 12, 14, 19 and 21-23 are rejected under the judicially created doctrine of anticipation-type double patenting as being anticipated by claims 1-13 of US patent **6,950,364** (Kim, "Self-Refresh Apparatus and Method), as shown in the following table. Although not all of the conflicting claims are exactly identical, they are extremely similar and are not patentably distinct from each other as explained in the "explanation" column of the table below:

6,950,364	10/608,575
1. A self-refresh apparatus comprising: an internal address counter for outputting internal address in response to an internal operation signal; a refresh controller for outputting the internal operation signal having a predetermined cycle in response to refresh command signals, and outputting a refresh operation signal having the predetermined cycle for selectively activating a bank when a partial bank refresh signal is applied for performing a partial array self-refresh on a bank; and a row address strobe generator for selectively activating the bank in response to the refresh operation signal.	1. (Currently amended) A self-refresh device, comprising: a command decoder for outputting a mode register set signal, a self-refresh signal and a refresh flag signal by decoding an externally inputted refresh command, a refresh counter for outputting a refresh request signal by performing a counting operation corresponding to a refresh cycle in response to the refresh flan signal; an internal address counter for counting and generating an internal address in response to the refresh flan signal and the refresh request signal; a partial array self-refresh decoder for generating a plurality of control signals for performing a partial array self-refresh operation in response to the mode register set signal, the self-refresh signal, and the internal address a row address strobe generator for controlling a row active signal for selectively activating one or more banks or a certain region in a selected single bank depending on states of the plurality of control signals when a refresh operation signal is activated.
2. The apparatus according to claim 1, further comprising: a command decoder for decoding a	2. (Currently amended) The device according to claim 1, further comprising:

refresh command inputted externally, and for outputting the refresh command signal and a mode register set signal; a refresh counter for outputting a signal having a predetermined cycle corresponding to a refresh rate in response to a self-refresh command signal out of the refresh command signals; a partial array self-refresh decoder for decoding and latching an extended mode register set code in response to the mode register set signal, and for selectively activating a plurality of control signals for performing a partial array self-refresh operation including the partial bank refresh signal by logically operating the latched code, in response to the self-refresh command signal; and a row address pre-decoder for decoding the internal address into a row address and for outputting the row address.	a row pre-decoder for outputting an external address as a row address in a normal mode, and outputting the internal address as the row address in a refresh mode.
3. The apparatus according to claim 2, wherein a plurality of control signals outputted from the partial array self-refresh decoder include a first control signal for selectively activating the row address strobe generator in response to a partial array self-refresh type, and second and third control signals for identifying the partial bank refresh signal.	6. (Currently amended) The device according to claim 1, wherein the partial array self-refresh decoder comprises: an extended mode register set decoder for outputting a register set control signal by decoding a bank selection address in response to the mode register set signal, The device according to claim 1, wherein the a plurality of address latches each for outputting register set address bit by latching an external address, in response to the register set control signal and the self-refresh signal when the mode register set signal is applied, and a partial array self-refresh controller for selectively activating the plurality of control signals by decoding the plurality of register set addresses depending on the internal address.
4. The apparatus according to claim 3, wherein the refresh controller controls the refresh operation signal depending on states of the most significant bit of the internal address when the second control signal is activated.	7. (Currently amended) The device according to claim 6, wherein the register set control signal is activated when the mode register set signal is activated, a most significant bit address of the bank selection address is high, and a second most significant bit of the bank selection address is low.
5. The apparatus according to claim 3, wherein the refresh controller controls the refresh operation signal depending on states of the second most significant bit of the internal address when the third control signal is activated.	12. (Currently amended) The device according to claim 6, wherein the partial array self-refresh controller outputs, the plurality of control signals by decoding the plurality of register set addresses and the plurality of inverted register set addresses.
6. The apparatus according to claim 3, wherein the partial array self-refresh decoder decodes a 3 least significant bits of applied address and selectively outputs one of the first, second and third control signals.	14. (Currently amended) The device according to claim 1, wherein the row address strobe generator generates the row active signal depending on a bank selection address and a normal operation signal ' in a normal mode, and generates the row active signal depending on the plurality of control signals and the refresh operation signal ' in a refresh mode.
7. The apparatus according to claim 3, wherein the row address strobe generator comprises: a first row address strobe generator for selectively activating the bank in response to the refresh operation signal in a refresh mode; and a second row address strobe generator for selectively activating the other banks in response to the first control signal and the refresh operation signal in a refresh mode.	19. (Original) The device according to claim 1, wherein the row address strobe generator is comprised to have the same number of the banks.
8. The apparatus according to claim 2, wherein the	21. (New) The device according to claim 6, wherein the

partial array self-refresh decoder comprises: an extended mode register set decoder for decoding bank selecting address in response to the mode register set signal, and for outputting a register set control signal; a plurality of address latches for decoding and latching the extended mode register set code in response to the register set control signal; and a partial array self-refresh controller for selectively outputting one of the first, second and third control signals by logically operating the latched address.	extended mode register set decoder sets up a code for performing a self-refresh operation on a cell array corresponding to a half of one bank when a partial array self-refresh operation is in a half of bank mode, and for performing a self-refresh operation on a cell array corresponding to a quarter of one bank when a partial array self-refresh operation is in a quarter of bank mode
9. The apparatus according to claim 1, wherein the refresh operation signal is selectively outputted in response to the partial bank refresh signal, and the internal operation signal is outputted in response to the signal having the predetermined cycle in a self-refresh mode regardless of the output of the refresh operation signal.	22. (New) The device according to claim 21, wherein when the partial array self-refresh operation is in a half of bank mode, the partial array self-refresh decoder activates a number of control signals corresponding to a quarter of the plurality of control signals until a most significant bit of address becomes high.
10. A self-refresh method for performing a partial array self-refresh operation on a semiconductor memory, wherein an internal address of the bank is continuously counted in a predetermined cycle corresponding to a refresh rate regardless of types of the partial array self-refresh when the partial array self-refresh operation is performed on a bank, and the bank is activated only when the internal address is counted to a predetermined address depending on types of the partial array self-refresh.	23. (New) The device according to claim 21 , wherein when the partial array self-refresh operation is in a quarter of bank mode, the partial array self-refresh decoder activates a number of control signals corresponding to a quarter of the plurality of control signals until at least one of two most significant bits of address becomes high.
11. A self-refresh method for performing a partial array self-refresh operation on a semiconductor memory in response to an extended mode register set code, comprising: the first step of activating a refresh operation signal for activating a bank and an internal operation signal for counting internal address when a partial array self-refresh command on a bank is applied; the second step of checking state change of a specific bit of the counted internal address depending on types of the partial array self-refresh; and the third step of continuously activating the internal operation signal in a predetermined cycle regardless of state change of the specific bit, and of inactivating the refresh operation signal when the state of the specific bit is changed.	
12. The method according to claim 11, wherein the second step checks state change of the most significant bit of the internal address when a self-refresh is performed on a half of a bank, and checks state change of the second most significant bit of the internal address when a self-refresh is performed on a quarter of the bank.	
13. The method according to claim 12, wherein the internal operation signal and the refresh operation signal are pulse signals having a predetermined	

| cycle corresponding to a refresh rate. | |

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7.   Claims 1-2, 6-7, 12, 14, 19 and 21-23 are rejected under 35 U.S.C. 102(e) as

being anticipated by Hwang et al. (US 6,590,822).

As to claim 1, Hwang et al. disclose **a self-refresh device** [System and method

for Performing Partial Array Self-Refresh Operation in a Semiconductor Memory

Device (title)], **comprising:**

a command decoder for outputting the mode register set signal, the self-refresh

signal and a refresh flag signal by decoding an externally inputted refresh

command [the memory device enters into a self-refresh mode in response to an

externally input command signal (column 2, lines 11-23); the command buffer, figure

16, 1601; column 13, lines 60-67; column 14, lines 1-4];

a refresh counter for outputting a refresh request signal by performing a

counting operation corresponding to a refresh cycle in response to the refresh

flag signal [cell data are amplified in connection with a self-refresh counter in Block1,

figure 15a (column 17, lines 1-7)];

an internal address counter for counting and generating an internal address in

response to the refresh flag signal and the refresh request signal [figure 16, 1605,

shows the internal address counters; column 2, lines 57-65];

a partial array self-refresh decoder [abstract; column 2, lines 50-57] **for generating**

a plurality of control signals for performing a partial array self-refresh operation

in response to the mode register set signal, the self-refresh signal, and the

internal address [a mode register setting signal PMRS is at a logic high level ...

(column 8, lines 27-48); column 3, lines 13-31]; **and**

a row address strobe generator [RAS, figure 4; column 7, lines 60-67] **for**

controlling a row active signal for selectively activating one or more banks or a

certain region in a selected single bank [1/2, 1/4, 1/8 or 1/16 of a selected memory

bank (column 2, lines 50-57)] **depending on states of the plurality of control**

signals when a refresh operation signal is activated [column 3, lines 5-12].

As to claim 2, Hwang et al. teach that **the device according to claim 1, further**

comprising:

a row pre-decoder for outputting an external address as a row address in a

normal mode, and outputting the internal address as the row address in a

refresh mode [the row address pre-decoder, figure 16, 1607; column 3, lines 45-50].

As to claim 6, Hwang et al. teach that **the device according to claim 1, wherein**

the partial array self-refresh decoder comprises:

an extended mode register set decoder for outputting a register set control

signal by decoding a bank selection address in response to the mode register

set signal [a mode register setting signal PMRS is at a logic high level ... (column 8, lines 27-48)];

a plurality of address latches each of which for outputting register set address bit by latching an external address, in response to the register set control signal and the self-refresh signal when the mode register set signal is applied [column 8, lines 3-18]; **and**

a partial array self-refresh controller for selectively activating the plurality of control signals by decoding the plurality of register set addresses depending on input of the internal address [the refresh controller, figure 2, 217; column 6, lines 39-45].

As to claim 7, Hwang et al. teach that **the device according to claim 6, wherein the register set control signal is activated when the mode register set signal is activated, a most significant bit address of the bank selection address is high, and a second most significant bit of the bank selection address is low** [a mode register setting signal PMRS is at a logic high level ... (column 8, lines 27-48)].

As to claim 12, Hwang et al. teach that **the partial array self-refresh controller outputs the plurality of control signals by decoding the plurality of register set addresses and the plurality of inverted register set addresses** [abstract; column 2, lines 50-57; a mode register setting signal PMRS is at a logic high level ... (column 8, lines 27-48); column 3, lines 13-31].

As to claim 14, Hwang et al. teach that **the device according to claim 1, wherein the row address strobe generator generates the row active signal**

depending on a bank selection address and a normal operation signal in a

normal mode, and generates the row active signal depending on the plurality of

control signals and the refresh operation signal activated in a refresh mode

[during a normal operating mode ..., column 2, lines 1-10; column 6, lines 10-22;

column 8, lines 3-17].

As to claim 19, Hwang et al. teach that the row address strobe generator is

comprised to have the same number of the banks [figure 16; column 3, lines 5-12].

As to claim 20, refer to "As to claim 1."

As to claim 21, Hwang et al. teach that the extended mode register set

decoder sets up a code for performing a self-refresh operation on a cell array

corresponding to a half of one bank when a partial array self-refresh operation is

in a half of bank mode, and for performing a self-refresh operation on a cell array

corresponding to a quarter of one bank when a partial array self-refresh

operation is in a quarter of bank mode [1/2, 1/4, 1/8 or 1/16 of a selected memory

bank (column 2, lines 50-57)].

As to claim 22, Hwang et al. teach that when the partial array self-refresh

operation is in a half of bank mode, the partial array self-refresh decoder

activates a number of control signals corresponding to a quarter of the plurality

of control signals until a most significant bit of address becomes high [1/2, 1/4,

1/8 or 1/16 of a selected memory bank (column 2, lines 50-57)].

As to claim 23, Hwang et al. teach that when the partial array self-refresh

operation is in a quarter of bank mode, the partial array self-refresh decoder

activates a number of control signals corresponding to a quarter of the plurality

of control signals until at least one of two most significant bits of address

becomes high [1/2, 1/4, 1/8 or 1/16 of a selected memory bank (column 2, lines 50-

57)].

Allowable Subject Matter

3.   Claims 8-11, 13 and 15-18 are objected to as being dependent upon a rejected

base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims and if able to overcome the

obviousness-type double patenting rejection in view of US patent **6,950,364**.

8.   ### Related Prior Art

The following list of prior art is considered to be pertinent to applicant's invention,

but not relied upon for claim analysis conducted above.

- Tsern et al., (US 6,345,009), "Apparatus and Method for Refreshing Subsets of

    Memory Devices in a Memory System."

- Jung, (US 6,137,742), "Semiconductor Memory Device Having Self-Refresh

    Control Circuit."

- Seyyedy, (US 5,818,777), "Circuit for Implementing and Method for Initiating Slef-

    Refresh Mode."

Conclusion

9.   Claims 1-2, 6-7, 12, 14 and 19-23 are rejected as explained above.

Claims 8-11, 13 and 15-18 are objected to as being dependent upon a rejected

base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims, and if able to overcome the

anticipation-type double patenting rejection in view of US patent **6,950,364**.

10.   THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time
policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

11.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-

4244. The examiner can normally be reached on 8:30 - 5:00.

       If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

<div style="text-align:right">

Sheng-Jen Tsai
Examiner
Art Unit 2186

</div>

December 30, 2005

PIERRE BATAILLE
PRIMARY EXAMINER